REMARKS/ARGUMENTS

Claims 1-37 are pending. Claim 17 was amended and claims 38-46 have been added. Consequently, claims 1-46 are now pending.

The Examiner objected to claim 17 for being indefinite. Claim 17 has been amended to correct a typographical error.

Applicant acknowledges and appreciates the Examiner's indication that claims 6-9, 12-23, 27-31, and 35-37 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, new claim 38 incorporates the limitations of claims 1-3 and 5-**6**; new claim 39 incorporates the limitations of claims 1-4 and 10-**12**; new claim for incorporates the limitations of 1-2 and 19-**23**; new claim 41 incorporates the limitations of claims 24-**27**; new claim 42 incorporates the limitations of 24-25 and **28**; new claim 43 incorporates limitations of 24-25 and **29**; new claim 44 incorporates limitations of claims 32-33 and **35**; and new claim 45 incorporates the limitations of claims 32 and **36**.

In addition, new claim 46 has been added to more particularly claim the present invention. New claim 46 recites similar limitations of recited in claim 39 (e.g., a plurality of serial buses and transmitting and receiving circuits, a plurality of frames, and the absence of DC balance). However, claim 46 further recites that the serial buses are "framed within a backplane" and that the "frames includes one framing cycle and a plurality of data cycles, thereby reducing bus overhead and enabling said circuits to perform clock recovery." Support for the amendments may be found out the specification. For example, with respect to the backplane, see page 7, lines 22-23; with respect to reducing bus overhead, see page 7, line 1-4; with respect to clock recovery, see page 7, lines 20-22; page 8, line 18 to page 9, line 9, and page 10, lines 12-23. Accordingly, no new matter has been entered.

The Examiner rejected claims 1-4, 10, 24-26, and 32-34 under 35 USC §102(a) as being anticipated by Bastiani et al. Applicant respectfully disagrees.

The present invention provides a Framed Packet Bus (FPB) that improves the bus data utilization rate between two devices that desire to communicate and transport data to and from one another, such as semiconductor chips, that are in close proximity sharing the same ground, or between components in a printed circuit card in a chassis. For instance, this is done by, among other things, relaxing the requirement for DC balance. Thus, one characteristic of the protocol employed by the devices utilizing the FPB of the present invention is the absence of a guarantee of DC balance in the digital bits transmitted and received by the devices.

According to the present invention, two devices communicating over a serial bus utilize a data format in which data is sent by the devices in a series of frames comprising a block or plurality of bits (also termed a "cycle"), which may be framing cycles, which contain control data useful for framed packet communication, or the cycles may be data cycles, which contain the information of interest between the communicating devices.

The devices comprise any circuits that communicate to and from one another serially and where, due to proximity, the requirement for DC balance may be safely relaxed. The devices 20 and 22 may include pure photonic and optical switches as well, where there is by definition no requirement for DC balance. Because of the relaxation of the DC balance, the devices are generally contained within and grounded to a single common device or housing (e.g., such as a backplane).

Using the data format of the present invention it is estimated that the bus data utilization rises from less than 80% to approximately 95%, and conversely the bus overhead falls from over 20% to about 5%, contingent on the quality of the clock oscillator and clock synchronization circuit used in the implementation. The relaxation of the DC balance requirement in the present

invention stands in marked contrast to prior implementations of serial bus protocols, such as an 8B/10B encoder.

Applicant is respectfully submitted that Bastiani discloses a protocol for communication between host computers and peripheral devices that utilizes a packet format that fails to teach or suggest the improved protocol of the present invention as claimed.

To support the rejection of claim 1, the Examiner states "the inventor [Bastiani] does not disclose a pattern of bit generation to maintain a DC balance when formatting the digital bits. Hence there is no requirement for the bits to be formatted DC balance."

Although Bastiani does not explicitly state that his protocol is DC balanced, figure 41, block 372 is described in column 48, line 63 as an encoder/decoder that converts bit streams to encoded data and strobe signals and vice versa. Applicant believes that this implies an 8B/10B type of encoding, which generally yields DC balance at a cost of extra bits. This also implies that DC balance is important due to the complemented control fields and DC balanced sync character.

In addition, Bastiani discloses a protocol between two *external* devices, in which case it is believed DC balance is necessary for the protocol to work, otherwise one needs a clear way to tie the ground between the devices very cleanly. In other words, it is believed in order for Bastiani to work, either DC balance is needed or a ground cable. The protocol of present invention does not have this limitation because the two devices communicating over the serial bus are internal to the same structure (e.g., the same backplane, as in claim 45) where there is control over the ground planes and distribution.

Another difference is that a frame per Bastiani delineates a single message. A frame in the present invention is a physical transmission requirement that enables clock recovery and provides for back channel error management if desired. A "frame" is used for entirely different purpose than Bastiani's sync character. Fundamentally, Bastiani discloses a message protocol,

while the present invention provides a physical bus protocol on which a message protocol of choice could be layered. In other words, the present invention provides a physical layer protocol that supports link layer needs, whereas Bastiani provides more of a link layer protocol that shows some possible physical implementation (which varies from implementation of the present invention).

Due to these protocol differences, Bastiani provides error checking within a message at the message protocol level, whereas the protocol of present invention is not tied to individual messages, but rather is tied to the entire bit stream. Furthermore, whereas Bastiani's protocol requires the sending of a strobe or clock signal over the serial bus and heavy grounding, the present invention recovers clocking from the very nature of the physical framing on the bus, as recited in claim 46, such that the presence of strobe or clock signals is not required. And extra grounding in the present invention is unnecessary for internal chassis communications where a ground plane is common.

In view of the foregoing, it is submitted that claims 1-46 are allowable over the cited references. Accordingly, Applicant respectfully requests reconsideration and passage to issue of claims 1-46 as now presented.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

SAWYER LAW GROUP LLP

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Stephen G. Sullivan
Attorney for Applicant(s)
Reg. No. 38,329
(650) 493-4540